DFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Ferruccio Frisina, Giuseppe Ferla, Angelo Magri', Dario Salinas

Title: **MOS POWER DEVICE WITH HIGH INTEGRATION DENSITY AND MANUFACTURING PROCESS THEREOF**

Serial No.: 10/763,818

Filing Date: January 23, 2004

Attorney Docket No.: 2110-83-3

CERTIFICATE OF MAILING

I hereby certify that this paper or fee is being deposited with the United States Postal Service as First Class Mail addressed to Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450 on this 25th day of July, 2005 by

Signature

RESPONSE TO RESTRICTION REQUIREMENT

July 25, 2005

TO THE COMMISSIONER FOR PATENTS:

This communication is in response to the Office Action dated June 24, 2005 in which the Examiner restricted the pending claims in the present patent application.

The Examiner has restricted the claims into two groups: claims 1 – 7 and 13 - 20 (Group I), and claims 8 - 12 and 21 - 29 (Group II). As discussed below, the Applicants respectfully traverse the restriction requirement on the grounds that the Examiner can search and examine the entire application without serious burden. Although the

Applicants traverse the restriction requirement as discussed below, they provisionally elect to prosecute Group I claims 1 – 7 and 13 - 20 if the Examiner does not withdraw the restriction requirement.

According to MPEP § 803, if the Examiner can search and examine the application without serious burden, then he/she **MUST** examine the application on the merits even though it includes claims to independent or distinct inventions. As discussed below, because claims 1 – 29 recite similar subject matter, the Examiner can perform a single search and examination that will cover all of the claims. Consequently, the Examiner can search and examine the application without serious burden, and, therefore, **MUST** examine all of the claims 1 – 29 together.

More specifically, claim 1 recites:

1. A MOS power device, comprising:

a body of semiconductor material having a first conductivity type and a surface;

at least two gate regions, of semiconductor material, arranged on top of said surface of said body and insulated from said body by gate-insulation regions, said gate regions being arranged at a distance from one another and delimiting between them a window having a given width;

a body region housed in said body, underneath said window, said body region having a second conductivity type and a first doping level;

a conductive region, accommodated in said body region and facing said surface, said conductive region having said first conductivity type and a second doping level;

a dielectric region covering said gate regions; and

a metal region extending on top of said dielectric region and being in electrical contact with said body and conductive regions;

characterized by:

first contact regions, distinct from said body region, extending from said

surface through said conductive region as far as said body region; and

second contact regions, extending in said conductive region and having said first conductivity type and a third doping level greater than said second doping level, said second contact regions extending at the side of said first contact regions;

in that said dielectric region further extends on top of said conductive region, at least piece-wise, throughout the width of said window and has first and second openings on top of said first and, respectively, second contact regions,

and in that said metal region extends through said first and second openings and is in direct electrical contact with said first and second contact regions.

Claim 8 recites:

8. A process for manufacturing a MOS power device, comprising the steps of:

providing a body of semiconductor material having a first conductivity type and a surface;

forming at least two gate regions, of semiconductor material, on top of said surface of said body and insulated from said body by gate-insulation regions, said gate regions being arranged at a distance from one another and delimiting between them a window;

forming, in said body, underneath said window, a body region having a second conductivity type and a first doping level;

forming, in said body region, a conductive region having said first conductivity type and a second doping level;

covering said gate regions and said surface, on top of said conductive region, with a dielectric region;

forming first and second openings in said dielectric region inside said window;

forming first contact regions, distinct from said body region and extending underneath said first openings and through said conductive region as far as said body region;

forming, in said conductive region underneath said second openings, second contact regions having said first conductivity type and a third doping level greater than said second doping level; and

forming a metal region on top of said dielectric region, said metal region extending through said first and second openings and being in direct electrical contact with said first and second contact regions.

Claim 13 recites:

13. A MOS power device including a body structure forming a drain region of the device, a body region formed in the body structure, a source region formed in the body region, and a two gate regions each formed adjacent and insulated from the body region, the device comprising:

at least one body contact region formed in the source region and extending through the source region to the body region, each body contact region having a first conductivity type and the body region having the first conductivity type, and each body contact region being more heavily doped than the body region;

at least one source contact region formed in the source region, each source contact region having a second conductivity type and the source region having the second conductivity type, and each source contact region being more heavily doped than the source region; and

a source contact region formed on the body and source contact regions.

Claim 19 recites:

19. An electronic system including a MOS power device having a body structure forming a drain region of the device, a body region formed in the body structure, a source region formed in the body region, and a two gate regions each formed adjacent and insulated from the body region, the MOS power device including,

at least one body contact region formed in the source region and extending through the source region to the body region, each body contact region having a first conductivity type and the body region having the first conductivity type, and each body contact region being more heavily doped than the body region;

at least one source contact region formed in the source region, each source contact region having a second conductivity type and the source region having the second conductivity type, and each source contact region being more heavily doped than the source region; and

a source contact region formed on the body and source contact regions.

Claim 21 recites:

21. A method of forming a MOS power device in a body structure having a first conductivity type, the method comprising:

forming a body region in the body structure, the body region having a second conductivity type;

forming a source region in the body region, the source region having the first conductivity type;

forming two gate regions adjacent the source and body regions and insulated from the source and body regions, an opening being defined between the two gate regions and at least a portion of the source region being exposed in the opening;

forming in the exposed portion of the source region at least one body contact region, each body contact region having the second conductivity type and extending through the source region to the body region, and each body contact region being more heavily doped than the body region; and

forming in the exposed portion of the source region at least one source contact region, each source contact region having the first conductivity type and being more heavily doped than the source region.

Claim 26 recites:

26. A method of forming a MOS power device in a body structure having a first conductivity type, the method comprising:

forming a body region in the body structure, the body region having a second conductivity type;

forming a source region in the body region, the source region having the first conductivity type;

forming two gate regions adjacent the source and body regions and insulated from the source and body regions, an opening being defined between the two gate regions and at least a portion of the source region being exposed in the opening;

removing portions of the exposed portion of the source region to form at least one body contact region; and

forming in the exposed portion of the source region at least one source contact region, each source contact region having the first conductivity type and being more heavily doped than the source region.

The Examiner can perform a single search for claims 1 – 29. Furthermore, because these claims recite related subject matter, examination of these claims will involve similar analyses. Therefore, it is only slightly more burdensome for the Examiner to search and examine claims 1 – 29 than it would be for him/her to search and examine the provisionally elected Group I claims 1 – 7 and 13-20. Consequently, because there is no serious burden on the Examiner to search and examine all of the claims 1 – 29, the **restriction is improper**. Therefore, the Examiner **MUST** withdraw the restriction and examine all of the claims.

Therefore, as discussed above, the Applicants respectfully request the Examiner to withdraw the restriction requirement and to examine all of the claims 1 - 29.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicants' attorney, Paul F. Rusyn, at (425) 455-5575. In the event an additional fee is due for this Response, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP

Paul F. Rusyn
Attorney for Applicant
Registration No. 42,118
155 - 108th Avenue NE, Suite. 350
Bellevue, WA 98004-5973
(425) 455-5575

Enclosure:
Return Postcard